WIDE-BAND MONOLITHIC GaAs PHASE DETECTOR FOR HOMODYNE RECEPTION

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Abstract

A multipurpose, 0,04 - 4 GHz, monolithic GaAs detector circuit has been fabricated. It shows a sensitivity of 2.5 V/rad with a DC offset of 300 mV for a differential dynamic range of 8 V. It has been successfully tested as a phase detector in a homodyne receiver over L and S bands.

INTRODUCTION

Homodyne reception is an attractive alternative for telecommunication systems. The synchronous detection is performed at the RF frequency, which greatly simplifies the receiver due to the absence of IF circuitry.

One of the critical part of the phase loop of the receiver is the phase detector which is basicaly a multiplier circuit. This type of device can also perform as a mixer in heterodyne receivers.

For cost effectiveness and multipurpose use, a very wide-band design has been investigated. The fabricated device covers all the bands from VHF to S band (i.e. from 40 MHz up to 4 GHz).

To achieve this wide-band performance a "high impedance" (or "voltage") type of operation, excluding inductive elements has been used. Moreover, this solution leads to a drastic increase in real estate efficiency.

The circuit consists of an analog multiplier with an input splitter-amplifier in front followed by an output-buffer amplifier (fig. 1).

MULTIPLIER

A double balance mixer has been used to reach a low level of intermodulation distortion and a low DC offset. Due to the balanced structure, the LO signal is rejected at the drain of all 6 transistors which form the active part of the circuit. In this way no contribution of the drain non-linearities occur on the intermodulation distortion. The simulation of the mixer behaviour has been performed using a time domain analysis and a non-linear model of the MESFET developed in our laboratory. The calculated conversion gain is 5 dB and the third order intercept point, IP_3 = 15 dBm.

INPUT SPLITTER

A differential amplifier performs the active splitting.

To ensure simultaneously high gain (low RF load conductance) and low drain supply voltage (high D.C. load conductance) an active load has been preferred. Unfortunately, as the D.C. dynamic conductance is even lower than the high frequency conductance , accurate control of the biasing of three series transistors is quite intricate. To avoid this difficulty a new type of active load (1) has been used. It consists of a FET with the gate biased, through a high value resistance (10 kΩ) to a fixed voltage of approximately 2/3 V_{DD}. At D.C. the circuit performs as a cascode stage, while at high frequency it acts as a classical (through Cgs) active loads with gate connected to source.

To increase the bandwidth of the amplifier an active feedback is used.

The calculated gain of the input stage is 6 dB.

OUTPUT BUFFER AMPLIFIER

Two intermediate small size common drain stage drive a 50Ω output buffer amplifier consisting of 4 cross coupled FET's (2).

Since the voltage gain A of the inverting (common source) and non-inverting (common drain) transistors are the same :

$$1/A = 1 + 2\,(g_{ds} + g_{load})/g_m$$

This differential push-pull amplifier presents extremely well balanced outputs into 50Ω , thus compensating for some unbalance between the mixer outputs. Moreover, as compared with usual common drain buffer stages with the same output impedance and the same total FET's widths, this novel configuration provides 6 dB gain improvement (that is to say 1 dB gain instead of 5 dB loss).

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FABRICATION

The complete phase detector circuit (fig. 2) contains 26 0.8 µm MESFET's over 0.4 mm^2 area (fig. 3). Except for the output stage, the width of transistors is between 10 and 40 µm.

A simple process, without via holes and requiring only seven mask levels has been employed. A fabrication yield of 70 % has been obtained.

MEASUREMENTS

Fig. 4 shows the mixer conversion gain versus RF. It is 12.5 dB at low frequency and 6 dB at 4.5 GHz. The third order intercept point is 15 dBm over all the band. The IF bandwidth is DC to 250 MHz. All these results are within 5 % of the CAD simulation.

The DC offset has been measured to be less than 300 mV for a differential dynamic range of 8 V. These good results show the accuracy of the balance obtained in the circuit even at high frequency.

The sensitivity of the phase detector is 2.5 V/rad.

The performances of the circuit have been tested in a homodyne receiver with a static bandwidth of the PLL of 7 MHz.

Fig. 5 shows the output signal spectrum for a 2 GHz signal modulated at 100 KHz with a modulation index of 0.25.

CONCLUSION

A wide-band monolithic GaAs mixer/phase detector device has been fabricated covering the whole VHF to S band frequency range. In a homodyne detection PLL, it shows the same quality at microwave frequency as Si phase detectors at a few MHz. Due to its low intermodulation distorsion it is very suitable for high "spec" heterodyne receivers.

The voltage gain approach, combined with monolithic techniques, is confirmed to be a promising alternative at microwave frequency. It allows the fabrication of very broad band circuits and leads to a real estate efficiency much higher than that of classical microwave solutions.

With 0.8 µm gate length D type MESFET's the present limit of this technique is around 4-5 GHz. As a matter of fact, it will be increased up to 10 GHz if devices with higher f_T's ($\sim$40 GHz) are used.

References :

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Wide band, High Gain, Small Size Monolithic GaAs FET amplifiers
Int. M. W. Symposium 1983

2 Thierry Ducourant
"Circuit amplificateur différentiel régénérateur de signaux complémentaires de faible amplitude".
French patent, 1986

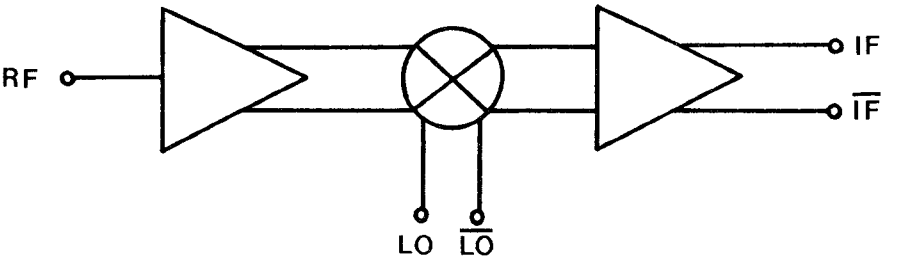

Figure 1 : Block diagram of the circuit

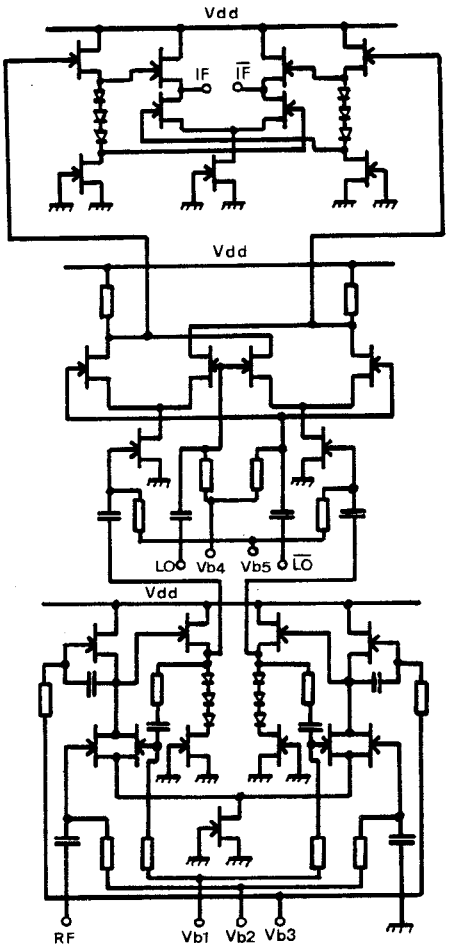

Figure 2 : Schematic of the complete circuit

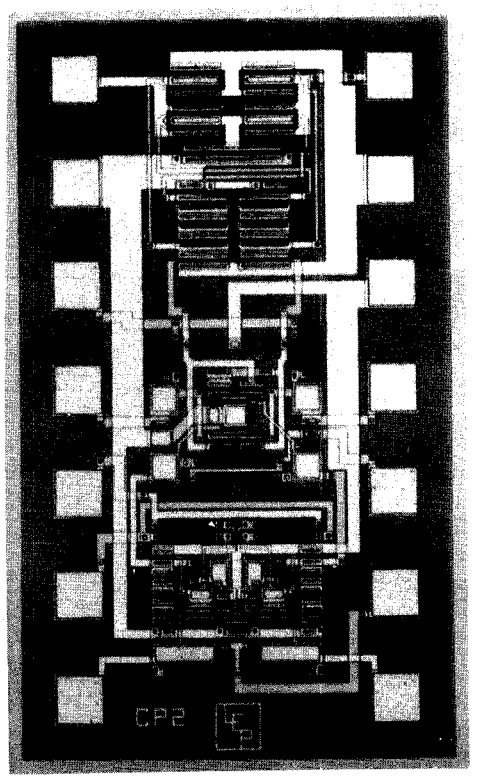

Figure 3 : Microphotograph of the circuit

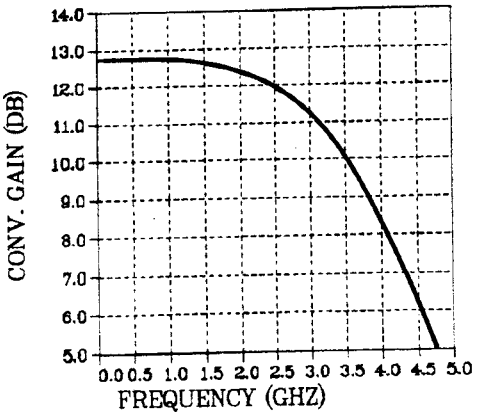

Figure 4 : Frequency response curve of the phase detector

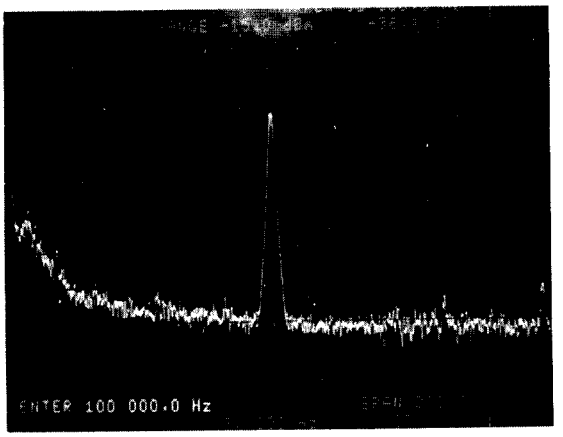

Figure 5 : Output homodyne reception spectrum for a 2 GHz input signal